

REMARKS

In the Office Action, Claims 1-26 are pending, were examined and stand rejected. In this Response, Claims 1, 7, 15 and 21 are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-26 in view of the following remarks.

I. Double Patenting Rejection

The Examiner rejects Applicants' invention under the provisional obviousness-type double patenting rejection as not patentably distinct from the claimed inventions of co-pending U.S. Patent Application No. 10/781,512 although the conflicting claims are not identical. Applicants hold in abeyance this rejection until such time as the claims on which the rejection is premised are granted.

II. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claims 1-19 and 21-26 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,158,018 to Bernasconi et al. ("Bernasconi"). Applicants respectfully traverse this rejection.

Regarding Claim 1, Claim 1 is amended to recite the following claim feature, which is neither disclosed, taught nor suggested by Bernasconi:

a control logic coupled to the trigger-matching logic to select a set of instructions upon detection of at least one matched trigger condition and to execute operations as specified by the selected set of instructions to modify the captured incoming request cycle prior to transmission to a downstream destination device, wherein the set of instructions is selected based on the at least one matched trigger condition. (Emphasis added.)

The above-recited feature of amended Claim 1 now recites that the control logic executes operations as specified by the selected instruction set to modify the captured incoming request cycle prior to transmission to a destination device. Regarding the term "request cycles," Applicant's specification describes two categories of such request cycles, including a write request cycle that is used to transport data from a host processor to an end-user device or a read request cycle that is used to read data from the end-user device. (See, pg. 1, ¶3 of Applicant's specification.) Applicant respectfully submits that current DSP program addresses provided by

bus 24 neither discloses, teaches or suggests the incoming request cycles referred to by amended Claim 1.

According to the Examiner, Bernasconi discloses the capture of an incoming cycle at col. 9, line 54, where according to the Examiner, Bernasconi teaches the current DSP program address corresponds to the Applicant incoming cycle. (See, pg. 5, ¶4 of the Office Action mailed April 21, 2006.) The passage alluded to by the Examiner refers to three phases of operations of integrated circuit 12, for example, as shown in FIG. 1 of Bernasconi. As disclosed by Bernasconi regarding the three phases of operation of device 12:

In particular, in one phase of operation, the DSP 16 receives its software program from the ROM 18 such as from section 18a thereof because that section of ROM 18 contains flawless software. In a second phase of DSP operation, a match is detected between the current DSP program address and a break address corresponding to the beginning of flawed DSP program software in the ROM 18 such as at section 18b thereof. At this stage, the patching circuitry 22 sends to the DSP 16 a branch op code followed by a branch address corresponding to the beginning of a block of corrected DSP program software in the RAM 20 such as in section 20b thereof. Therefore, in the third general phase of device operation, the DSP 16 fetches corrected DSP program software instructions from the RAM 20 such as section 20b thereof. (col. 9, lines 50-64.) (Emphasis added.)

Regarding the operation of device 12, the various components of device 12, as shown in FIG. 1, are described by Bernasconi as follows:

Bus 24 provides the current DSP program address from the embedded DSP (hereafter more simply referred to as “DSP”) to the patching circuitry 22, the ROM 18, and the RAM 20. Additionally, DSP program software stored in the ROM 18 is provided via bus 26, the patching circuitry 22, and bus 30 to the DSP 16. Similarly, corrected DSP program software stored in the RAM 20 such as section 20b of the RAM 20 is provided via bus 28, the patching circuitry 22, and bus 30 to the DSP 16. (col. 6, lines 15-23.) (Emphasis added.)

As indicated by the cited passage above, reference numeral “24” of FIG. 1 refers to a bus, which as taught by Bernasconi, provides the current DSP program address from the embedded DSP 16 to the patching circuitry 22, the ROM 18 and the RAM 20. (See, supra.) As further disclosed by Bernasconi, the DSP program address is compared against a break address to identify flawed DSP program software. (See, col. 9, lines 53-57.)

Applicant respectfully submits that the use current DSP program address provided by bus 24 from DSP 16 to patching circuitry 22, ROM 18 and RAM 20 to identify flawed DP program software neither teaches nor suggests the capture of an incoming request cycle received by an

I/O controller nor the modification of such cycle prior to transmission to a downstream destination device, as recited by amended Claim 1.

As mandated by case law, “Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.” Lindemann Maschinenfabrik v. American Hoist & Derrick (“Lindemann”), 730 F.2d 452, 1458 (Fed. Cir. 1994) (emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. Titanium Metals Corp. of American v. Banner (“Banner Titanium”), 778 F.2d 775, 777 (Fed. Cir. 1985).

Here, the Examiner has incorrectly equated the DSP program address, which is provided by bus 24 to patching circuitry 22, ROM 18 and RAM 20, with the incoming request cycle referred by amended Claim 1. However, to further illustrate the features of amended Claim 1, amended Claim 1 recites the capture of an incoming request cycle from an upstream device, as well as the modification of such captured incoming request prior to transmission to a downstream destination device, as performed by the control logic recited by amended Claim 1.

Accordingly, for at least the reasons provided above, Applicant respectfully submits that the Examiner is prohibited from relying on Bernasconi as an anticipatory reference, since Bernasconi fails to exactly disclose each and every element recited by amended Claim 1 and specifically, the capture of an incoming request cycle from an upstream device and modification of the captured incoming request cycle prior to transmission to a downstream destination device. Banner Titanium, *supra*. Hence, Applicant respectfully submits that Applicant’s amendment to Claim 1 prohibits the Examiner from illustrating that the single prior art reference disclosure of Bernasconi includes the presence of each and every element recited by amended Claim 1 and as arranged in amended Claim 1. Lindemann, *supra*.

Consequently, for at least the reasons provided above, Applicant respectfully submits that amended Claim 1 is patentable over Bernasconi, as well as the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of amended Claim 1.

Regarding Claims 2-6, Claims 2-6, based on their dependency from Claim 1, are also patentable over Bernasconi, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claims 2-6.

Regarding Claims 7 and 21, Claims 7 and 21 recite the following claim features, which are neither disclosed, taught nor suggested by Bernasconi or the references of record:

capturing an incoming request cycle from an upstream device;

...

executing the selected generated instructions sequentially to modify the captured incoming request cycle prior to transmission to a downstream destination device. (Emphasis added.)

Applicant respectfully submits that the above-recited features of amended Claim 7 and 21 are analogous to the previously-described features of amended Claim 1. Accordingly, Applicant's arguments provided above with regard to the §102(b) rejection of Claim 1 as unpatentable over Bernasconi equally apply to the Examiner's §102(b) rejection of Claims 7 and 21 as anticipated by Bernasconi.

Consequently, for at least the reasons provided above, Applicant respectfully submits that the Examiner is prohibited from relying on Bernasconi as an anticipatory reference, since Bernasconi fails to exactly disclose the capture of an incoming request cycle from an upstream device, as well as the execution of selected generated instructions sequentially to modify the captured incoming request cycle prior to transmission to a downstream destination device. Banner Titanium, *supra*. Hence, Applicant respectfully submits that Applicant's amendment to Claims 7 and 21 prohibit the Examiner from establishing a *prima facie* case of anticipation, since the single prior art reference disclosure of Bernasconi fails to include the presence of each and every element recited by amended Claims 7 and 11. Lindemann, *supra*.

Therefore, for at least the reasons provided above, Applicant respectfully submits that Claims 7 and 11, as amended, are patentable over Bernasconi, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claims 7 and 21.

Regarding Claims 8-14 and 22-26, Claims 8-14 and 22-26, based on their dependency from Claims 7 and 21, respectively, are also patentable over Bernasconi, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claims 8-14 and 22-26.

Regarding Claim 15, Claim 15 is amended to recite the following claim feature, which is neither disclosed, taught nor suggested by Bernasconi or the references of record:

an instruction execution unit to execute the set of instructions selected by the instruction select unit to modify the captured incoming request cycle prior to transmission to a downstream destination device. (Emphasis added.)

Applicant respectfully submits that the above-described feature of amended Claim 15 is analogous to the previously-recited feature of at least amended Claim 1. Consequently, Applicant's arguments provided above with regard to the §102(b) rejection of Claim 1 as anticipated by Bernasconi equally apply to the Examiner's §102(b) rejection of Claim 15, as anticipated by Bernasconi.

For at least the reasons provided above, Applicant respectfully submits that the Examiner is prohibited from relying on Bernasconi as an anticipatory reference, since Bernasconi fails to exactly disclose each and every element of amended Claim 15; specifically, the execution of selected instructions sequentially to modify the captured incoming request cycle prior to transmission to a downstream destination device. Banner Titanium, supra. Hence, Applicant respectfully submits that Applicant's amendments to Claim 15 prohibit the Examiner from establishing a *prima facie* case of anticipation, since the single prior art reference disclosure of Bernasconi fails to include the presence of each and every element recited by amended Claim 15. Lindemann, supra.

Therefore, for at least the reasons provided above, Applicant respectfully submits that Claim 15, as amended, is patentable over Bernasconi, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 15.

Regarding Claims 16-20, Claims 16-20, based on their dependency from Claim 15, are also patentable over Bernasconi, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claims 16-20.

III. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claim 20 under 35 U.S.C. §103(a) as being unpatentable over Bernasconi in view of U.S. Patent No. 5,966,547 to Hagan et al. ("Hagan"). Applicants respectfully traverse this rejection.

Regarding Claim 20, Claim 20 depends from Claim 15. As indicated above with regards to the §102(b) rejection of Claim 15, Bernasconi fails to exactly disclose each of the recited

features of amended Claim 15 and specifically, the instruction unit to execute the set of instructions selected by the instruction select unit to modify the captured incoming request cycle prior to transmission to a downstream destination device. Regarding the Examiner's citing of Hagan, Applicant respectfully submits that Hagan is directed to message passing between processors to communicate events or to assign tasks to be performed by the processors. Consequently, Applicant respectfully submits that the Examiner's citing of Hagan fails to recite the deficiencies of Bernasconi to teach or suggest at least the capture of an incoming request cycle from an upstream device and modification of such captured request cycle prior to transmission to a downstream device. Accordingly, Applicant respectfully submits that Claim 15 is patentable over the combination of Bernasconi in view of Hagan.

Therefore, for at least the reasons provided above, Applicant respectfully submits that Claim 20, based on its dependency from Claim 15, is also patentable over the combination of Bernasconi in view of Hagan. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 20.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: July 21, 2006

By: _____

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 21, 2006

Suzanne Johnston

July 21, 2006